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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,903	09/26/2001	Yoshikazu Kasuya	15.48/6066	9431

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,903	KASUYA, YOSHIKAZU	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,8-13 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-4,6,8-13 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *13* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' amendment filed On March 12, 2003 has been entered on March 25, 2003.

Therefore claims 1-4 and 9-13 as amended by the amendment and presently newly added claim 24 are currently pending in the application.

Claims 5,7 and 14 –23 have been cancelled by the amendment.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim*s 1-4, 6 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misra et al. (U.S. Patent No. 5,960,270, herein after Misra) previously applied . (for response to Applicants' arguments see section below).

With respect to claims 1 and 9, Misra describes a method of manufacturing a semiconductor device including the steps of : forming a gate dielectric layer on a semiconductor layer (fig. 10 # 105 on 102), forming a first conductive layer having a specified pattern on the gate dielectric layer (Fig. 11 # 108), forming sidewall spacers (insulation layers) on side walls of the first conductive layer (Fig. 12 # 114), forming a source region and a drain region in the semiconductor layer (fig. 12 # 118) depositing first insulating layer covering the first conductive layer and the side wall spacers (Fig. 14 # 120) the first insulation layer comprising a material different from that of the

sidewall insulation layers (105 oxide and 114-nitride) , planarizing the first insulation layer until an upper surface of the first conductive layer is exposed (fig. 15, planarize 120 to expose 108) , removing a part of the first conductive layer in a manner so that the gate dielectric layer is not exposed to thereby form a recessed section on the first conduction layer between the insulating layers (fig. 16, not exposing the gate oxide 125, col. 10 lines 1-16), to thereby from a recessed section on the conduction layer (fig. 19). It is noted that the figs. 19-22 show a second embodiment, however as stated in col. 10 lines 37-39, the steps describing the embodiment in figs. 10-16 are also used in the embodiment described in figs. 19-22 partially filling the recessed section with a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer. Forming a second insulation layer that fills the recessed section on the second conductive layer, the second insulation layer comprising a material different from that of first insulation layer (Misra fig. 14 # 120 of nitride the first insulating layer of oxide), etching the first insulation layer to form a first through hole that reaches the source region or the drain region (Misra fig. 17, col. 18 lines 17-23), forming a first contact layer in the first through hole. (Misra fig. 17, # 128 a col. 18 lines 18).

With respect to claim 2, wherein in the step (j) , the second insulation layer and the sidewall insulation layer compose a material that is more resistant to an etchant than the first insulation layer (Misra col. 10 lines 1-16, col. 6 lines 35-44)

With respect to claim 3, wherein the first conductive layer is formed from a material comprising silicon (Misra col. 9 line 31, layer 108 of polysilicon) and step h

includes the steps of depositing a metal layer .for siliciding the first conductive layer , on the first conductive layer (Misra col. 10 lines 42-45), siliciding the first conductive layer to form a silicide layer (Misra col. 10 lines 57-60).

With respect to claim 4, to the extent understood, wherein the method step includes:

Forming a third insulation layer on the first insulation layer and the second insulation layer (Misra fig. 16 # 122, col. 9 line 57); etching the third insulation layer to form a second through hole (Misra fig. 20), forming a second contact layer in the second through hole, wherein the second through hole overlaps the first through hole

With respect to claim 6, to the extent understood, wherein the first insulation layer comprises silicon oxide and the second insulation layer comprises silicon nitride . (Misra col. 9 line 26 and col. 9 lines 39-40).

With respect to claim 8, wherein the first insulation layer comprises silicon oxide and the sidewall insulation layers comprise silicon nitride . (Misra col. 9 line 26 and col. 9 lines 39-40).

With respect to claims 10 and 11, to the extent understood, repeat the steps of claims 1 and therefore are rejected for reasons set out under claim1 above.

With respect to claim 13, wherein the removing a part of the first conductive layer further includes removing a greater depth of the first concentration layer from a center region rather than from end regions adjacent to the sidewall insulation layers . (Misra fig. 7 etc.).

With respect to Claim 24, Misra describes a method of manufacturing a semiconductor device according to claim 9, wherein the first insulation layer comprises silicon oxide and the second insulation layer comprises silicon nitride. ((Misra col. 9 line 26 and col. 9 lines 39-40).

Response to Arguments

Applicant's arguments filed 3/1/2003 have been fully considered but they are not persuasive for the following reasons :

The following was also discussed by Mr. Raynes and Ex. Rao during their interview.

Applicants' first argument that Misra fails to teach " removing a part of the first conduction layer in a manner so that the gate dielectric layer is not exposed to thereby form a recessed section on the first conduction layer between the insulating layers " is not persuasive because MIsra in fig. 19 shows the following :

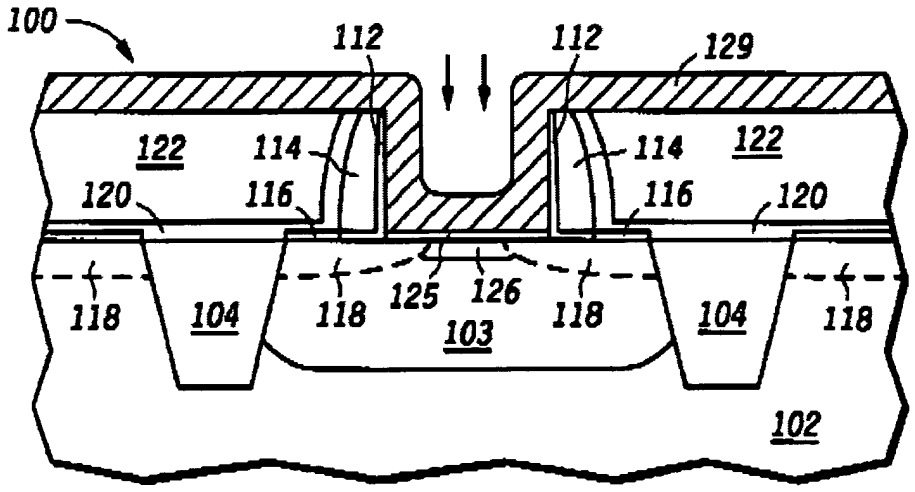

FIG.19

Applicants' second argument That Misra does not teach " filling a second conduction layer in the recessed section to form gate electrode that includes at least the first conductive layer in the recessed section to form gate electrode that includes at least the first conductive and second conductive layer " is not persuasive because Misra in figure 21 shows :

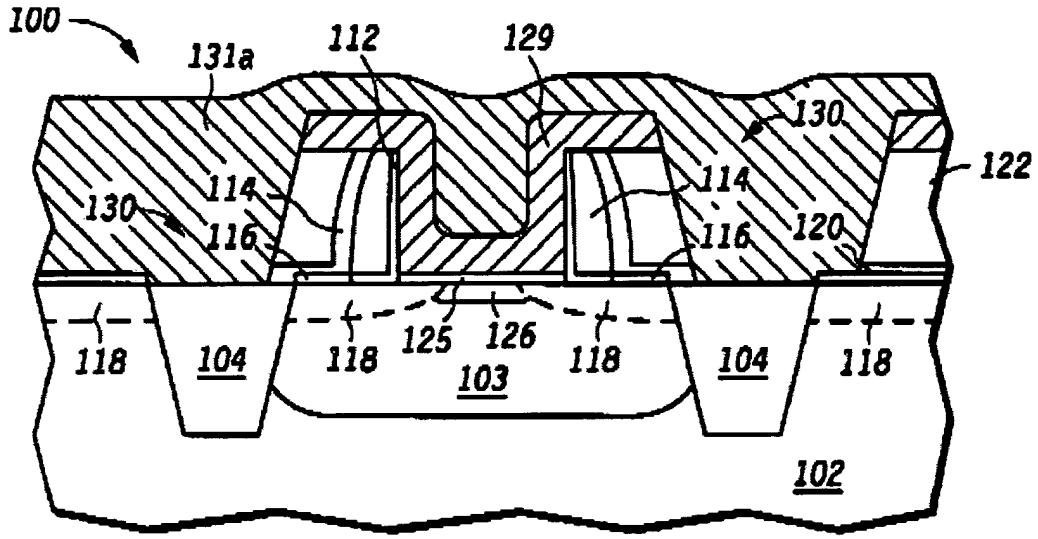

FIG.21

wherein layers 129 and 131a form the two layers.

Therefore claim 1 is not allowable.

Applicants' claim that dependent claims 2-4 and 6, 8 to 13 and 24 were allegedlly allowable because they depend on allegedly allowable claim 1.

However as shown claim1 is not allowable , therefore claims 2-4,6 and 8to 13 and 24 are also not allowable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-3926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 3067722.

Steven H. Rao

Patent Examiner

June 1, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800